

Claims

- [c1] 1. A photolithography process for Mask ROM coding, comprising: providing a substrate having an array of memory cells thereon; forming a first photoresist layer on the substrate covering the memory cells; performing a first exposure and development process to pattern the first photoresist layer into first line/space patterns; forming a second photoresist layer on the substrate covering the first line/space patterns; and performing a second exposure and development process to pattern the second photoresist layer into second line/space patterns having an orientation different from an orientation of the first line/space patterns, while a plurality of coding windows are defined by the first line/space patterns and the second line/space patterns.
- [c2] 2. The photolithography process of claim 1, wherein the first photoresist layer comprises a negative photoresist layer and the second photoresist layer comprises a positive photoresist layer.
- [c3] 3. The photolithography process of claim 1, wherein the orientation of the first line/space patterns is perpendicular to the orientation of the second line/space patterns.
- [c4] 4. The photolithography process of claim 1, wherein the first line/space patterns include a plurality of trenches having different lengths.
- [c5] 5. The photolithography process of claim 1, wherein the second line/space patterns comprise a plurality of linear patterns and linear spaces that are arranged regularly.
- [c6] 6. The photolithography process of claim 1, wherein the first exposure process and the second exposure process use off-axis illumination.
- [c7] 7. The photolithography process of claim 1, wherein the first exposure process and the second exposure process use an exposure light of 248nm.
- [c8] 8. The photolithography process of claim 1, wherein a coding window defined by the first line/space patterns and the second line/space patterns has a square shape.

- [c9] 9. The photolithography process of claim 8, wherein the square-shaped coding window has dimensions of $0.12\ \mu\text{m} \times 0.12\ \mu\text{m}$.
- [c10] 10. A photolithography process, comprising: forming a first photoresist layer on a substrate; performing a first exposure and development process to pattern the first photoresist layer into first line/space patterns; forming a second photoresist layer on the substrate covering the first line/space patterns; and performing a second exposure and development process to pattern the second photoresist layer into second line/space patterns having an orientation different from an orientation of the first line/space patterns, while a plurality of rectangle openings are defined by the first line/space patterns and the second line/space patterns.
- [c11] 11. The photolithography process of claim 10, wherein the first photoresist layer comprises a negative photoresist layer, and the second photoresist layer comprises a positive photoresist layer.
- [c12] 12. The photolithography process of claim 10, wherein the orientation of the first line/space patterns is perpendicular to an orientation of the second line/space patterns.
- [c13] 13. The photolithography process of claim 10, wherein the first line/space patterns include a plurality of trenches having different lengths.
- [c14] 14. The photolithography process of claim 10, wherein the second line/space patterns comprises a plurality of linear patterns and a plurality of linear spaces that are arranged regularly.
- [c15] 15. The photolithography process of claim 10, wherein a rectangle opening defined by the first line/space patterns and the second line/space patterns have a square shape.
- [c16] 16. The photolithography process of claim 10, further comprising performing a photoresist hardening process after the first photoresist layer is patterned into the first line/space patterns.
- [c17] 17. The photolithography process of claim 16, wherein the photoresist

hardening process comprises implanting Ar or N₂ ions with a dosage from about 1×10^{14} to about 3×10^{15} /cm² and an implanting energy from about 2KeV to about 50KeV.

[c18]

18. The photolithography process of claim 16, wherein the photoresist hardening process comprises a baking step at a temperature from about 100 ° C to about 150 ° C for a period from about 30 sec to about 180 sec.